FIG. 1

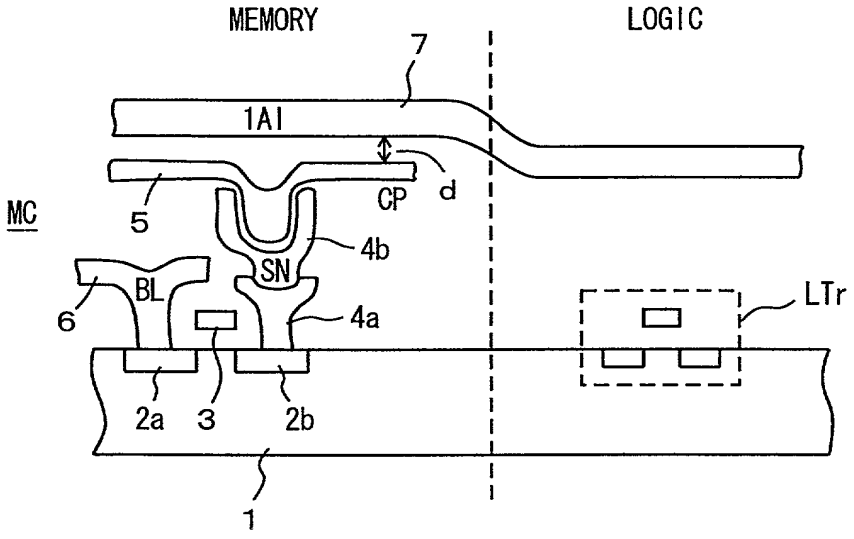
MEMORY
LOGIC
7
1AI
d
CP
MC
5
4b
SN
BL
6
4a
LTr
2a
3
2b
1

FIG. 2

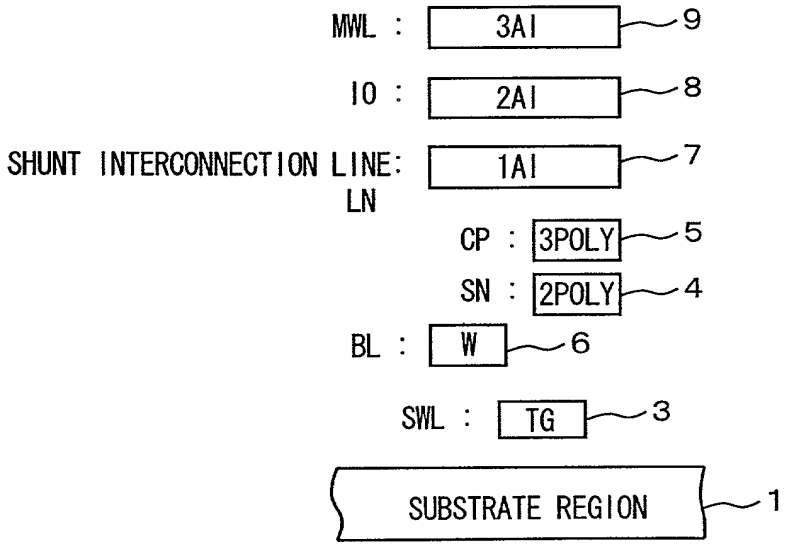
MWL : 3AI 9
IO : 2AI 8
SHUNT INTERCONNECTION LINE: LN 1AI 7
CP : 3POLY 5
SN : 2POLY 4
BL : W 6
SWL : TG 3
SUBSTRATE REGION 1

FIG. 3

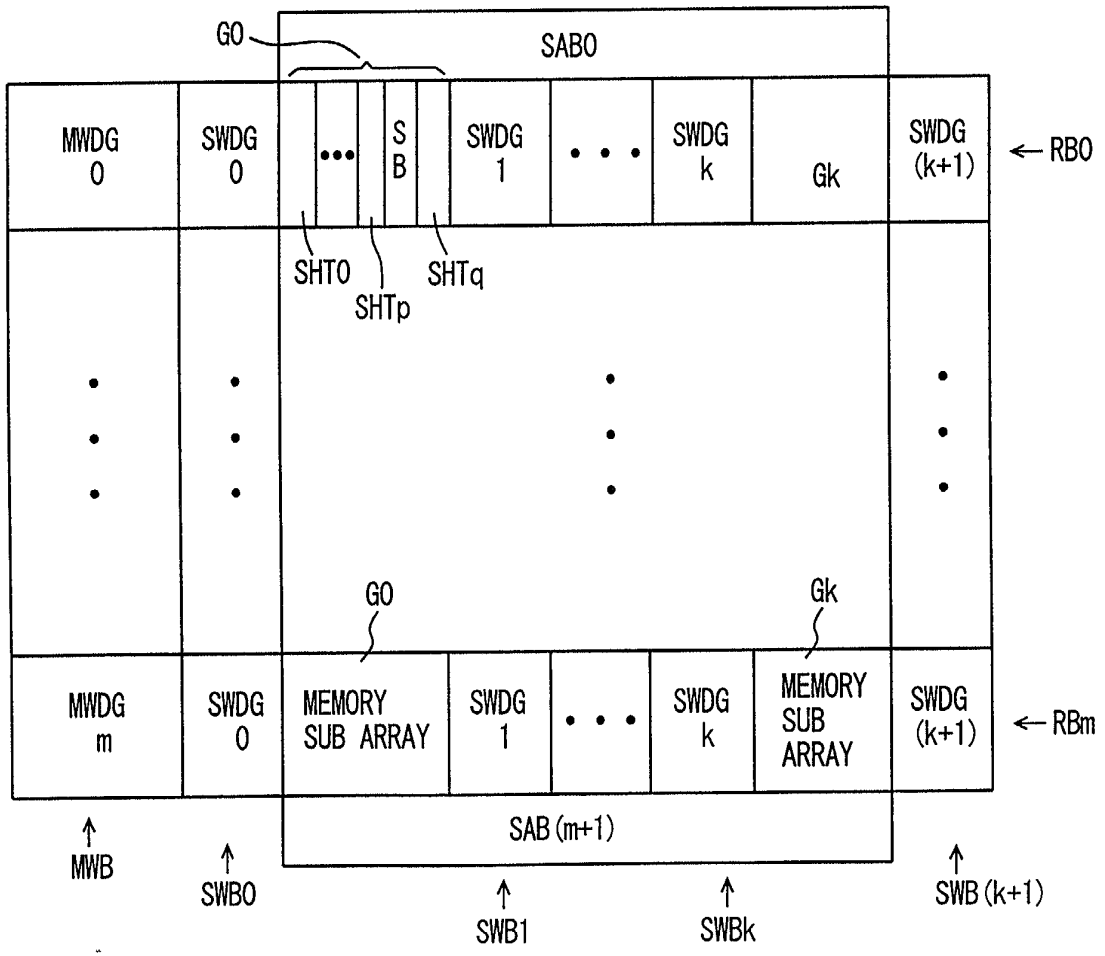
G0
SAB0
MWDG 0
SWDG 0
S B
SWDG 1
SWDG k
Gk
SWDG (k+1)
RB0
SHT0
SHTp
SHTq
G0
Gk
MWDG m
SWDG 0
MEMORY SUB ARRAY
SWDG 1
SWDG k
MEMORY SUB ARRAY
SWDG (k+1)
RBm
SAB (m+1)
MWB
SWB0
SWB1
SWBk
SWB (k+1)

FIG. 4A

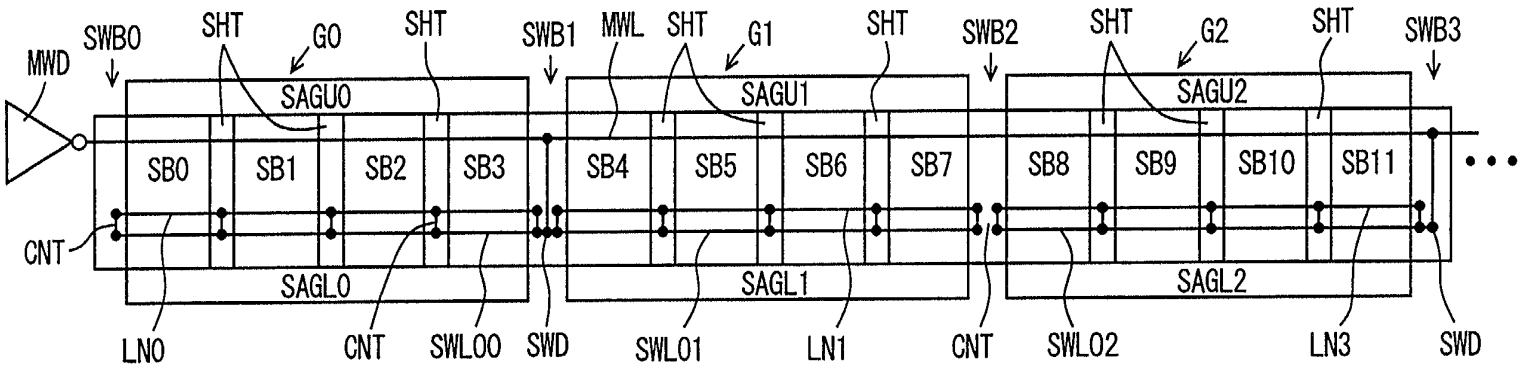
MWD
SWB0
SHT
G0
SHT
SWB1
MWL
SHT
G1
SHT
SWB2
SHT
G2
SHT
SWB3
SAGU0
SAGU1
SAGU2
SB0
SB1
SB2
SB3
SB4
SB5
SB6
SB7
SB8
SB9
SB10
SB11
CNT
SAGL0
SAGL1
SAGL2
LN0
CNT
SWL00
SWD
SWL01
LN1
CNT
SWL02
LN3
SWD

FIG. 4B

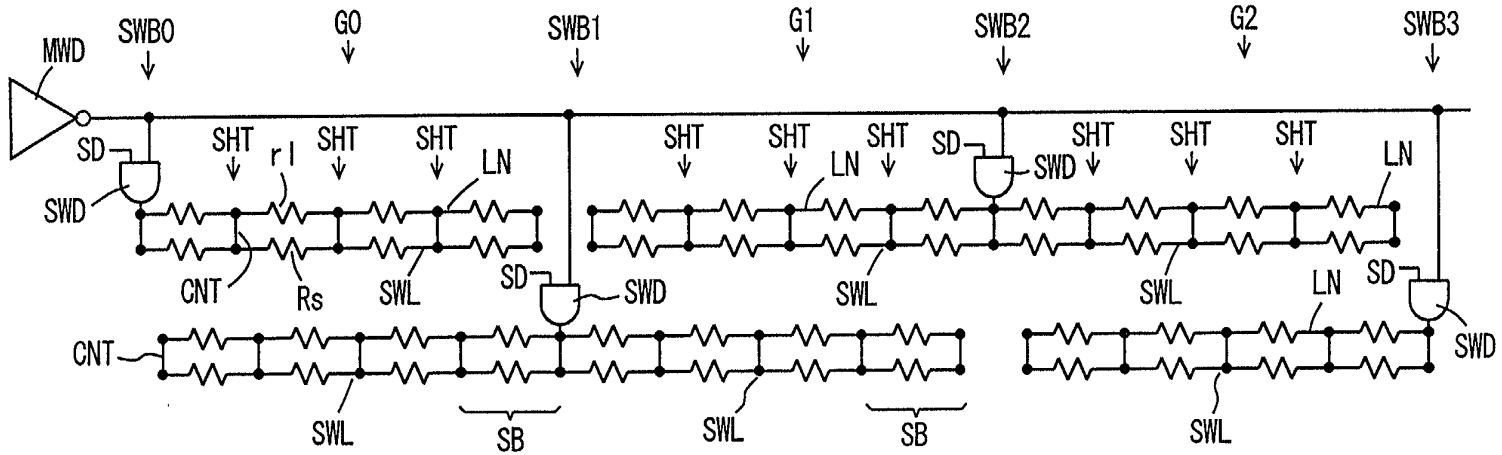
MWD
SWB0
G0
SWB1
G1
SWB2
G2
SWB3
SD
SHT
rl
SHT
SHT
LN
SWD
CNT
Rs
SWL
SD
SWD
SWL
SD
SWD
SWL
LN
SD
SWD
CNT
SWL
SB
SWL
SB
SWL

FIG. 5

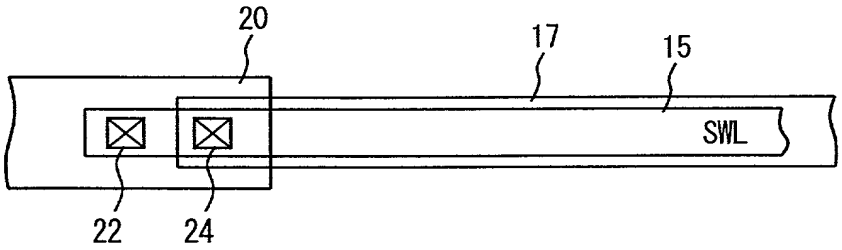

FIG. 6

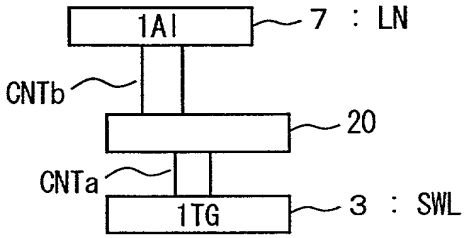

FIG. 7A

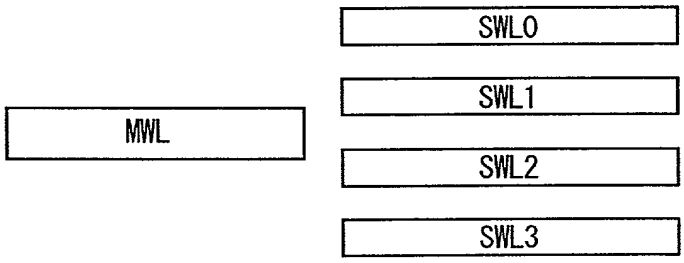

FIG. 7B

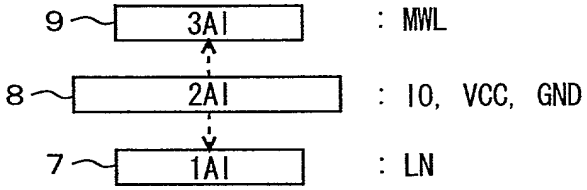

FIG. 8

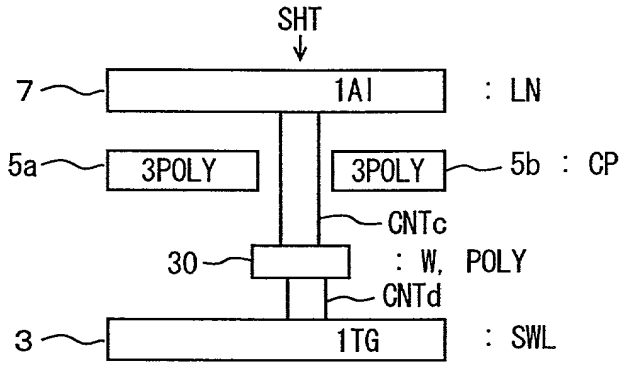

FIG. 9

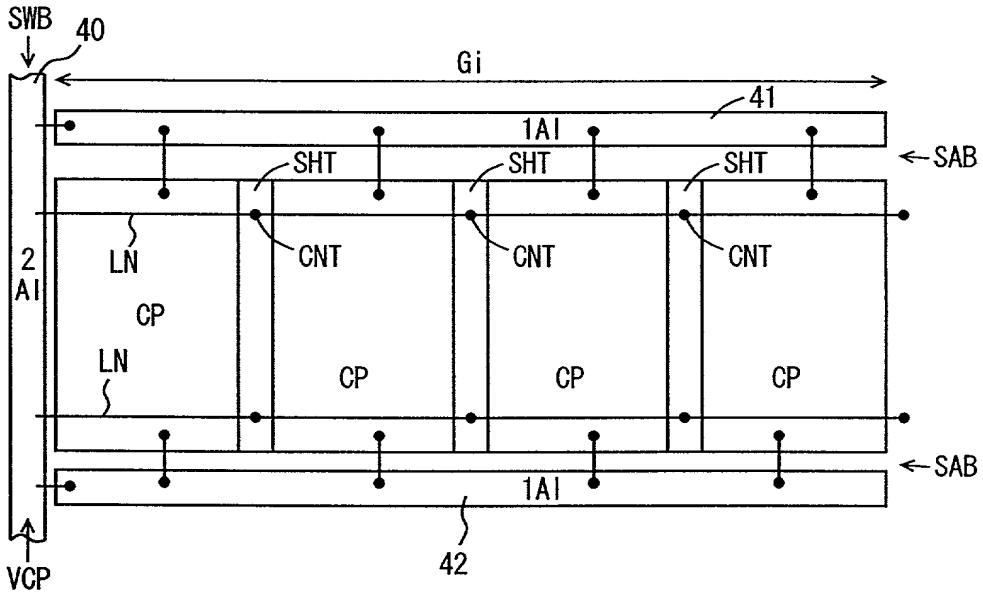

FIG. 10

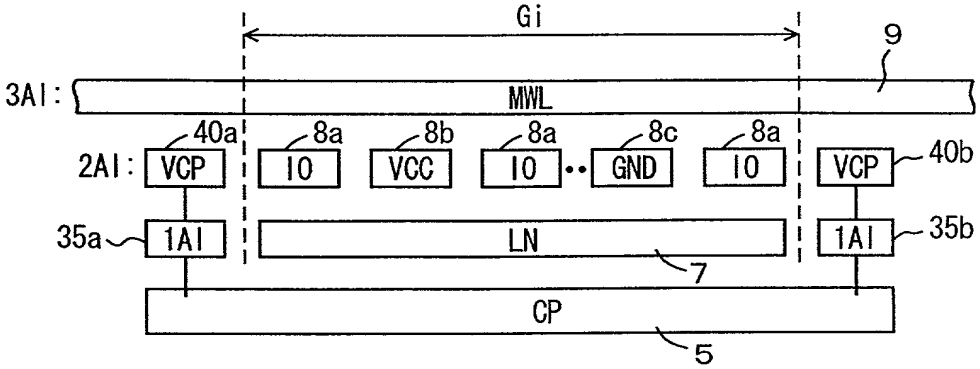

FIG. 11

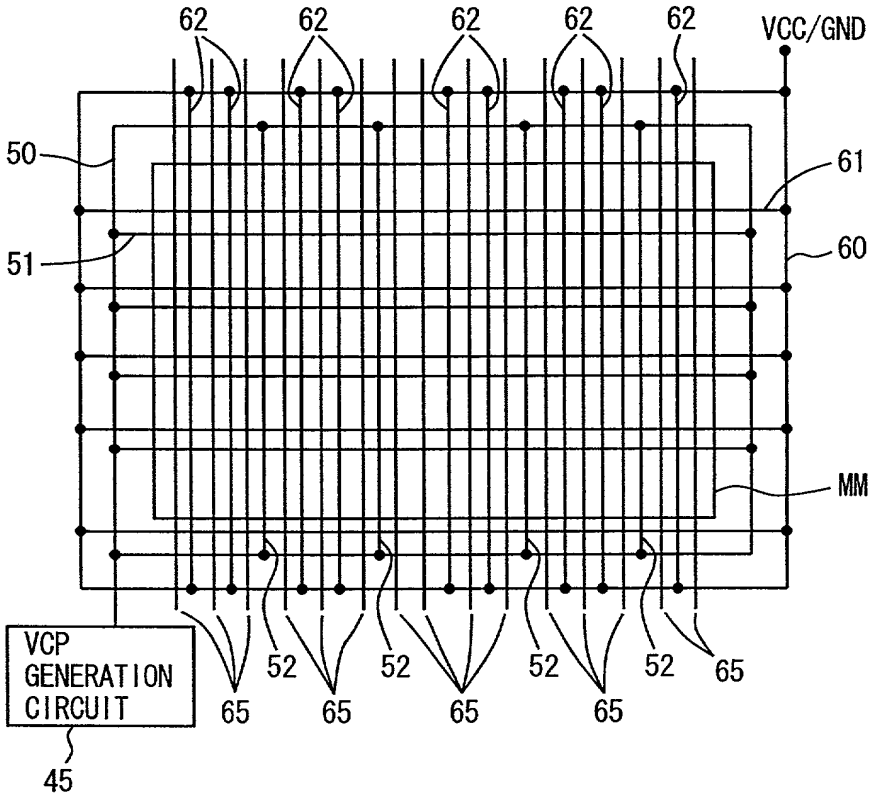

FIG. 12

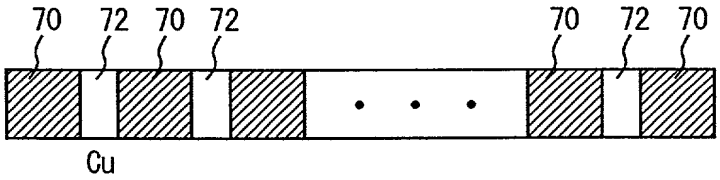

FIG. 13

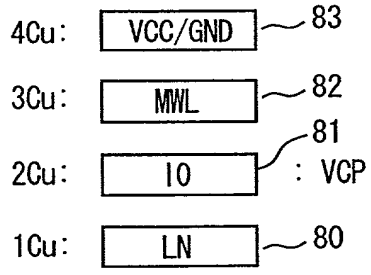

FIG. 14

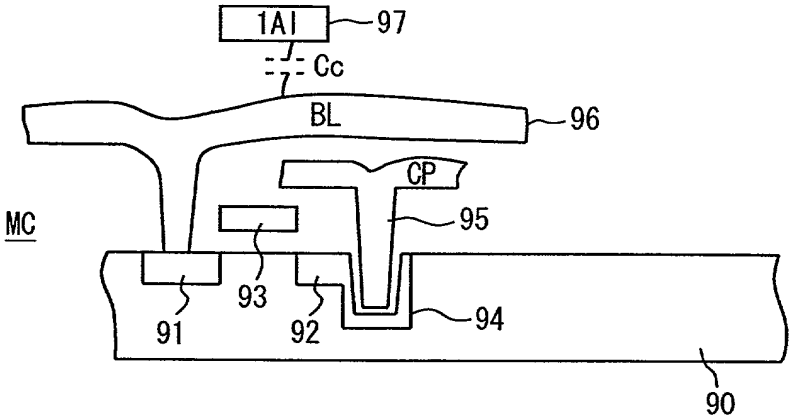
1A
97
Cc
BL
96
CP
MC
95
93
91
92
94
90

FIG. 15

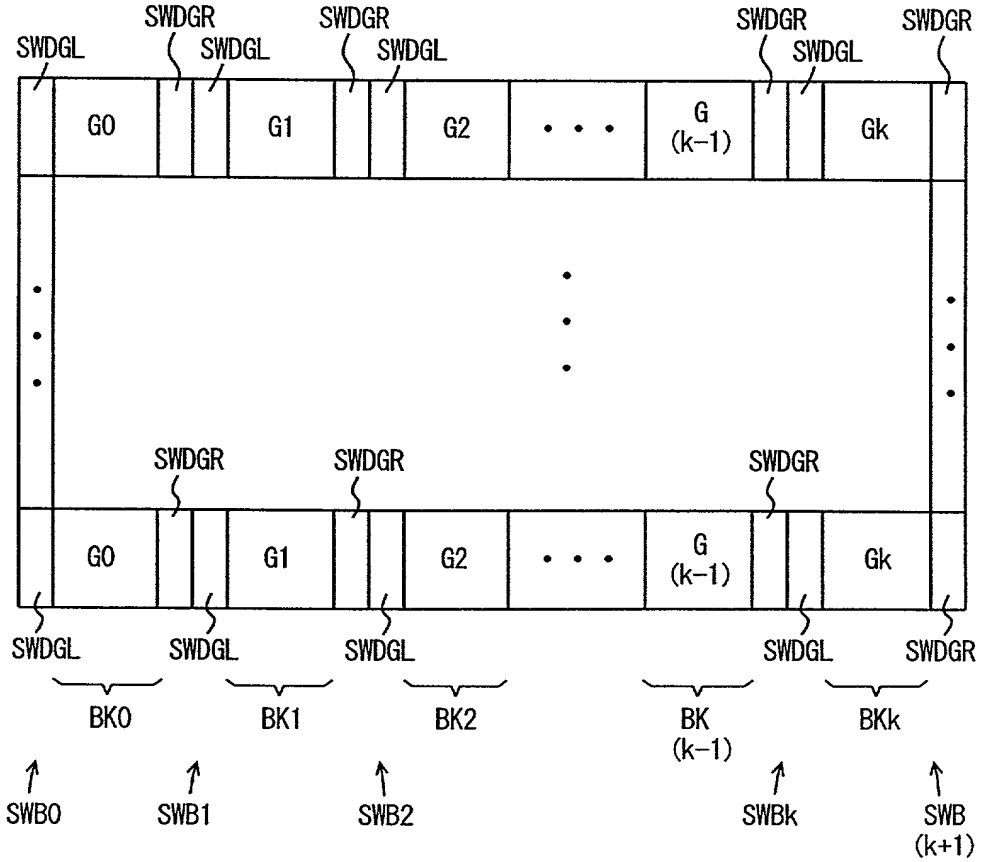
SWDGL
SWDGR
SWDGL
SWDGR
SWDGL
SWDGR
SWDGL
SWDGR
G0
G1
G2
G (k-1)
Gk
SWDGR
SWDGR
SWDGR
G0
G1
G2
G (k-1)
Gk
SWDGL
SWDGL
SWDGL
SWDGL
SWDGR
BK0
BK1
BK2
BK (k-1)
BKk
SWB0
SWB1
SWB2
SWBk
SWB (k+1)

FIG. 16A

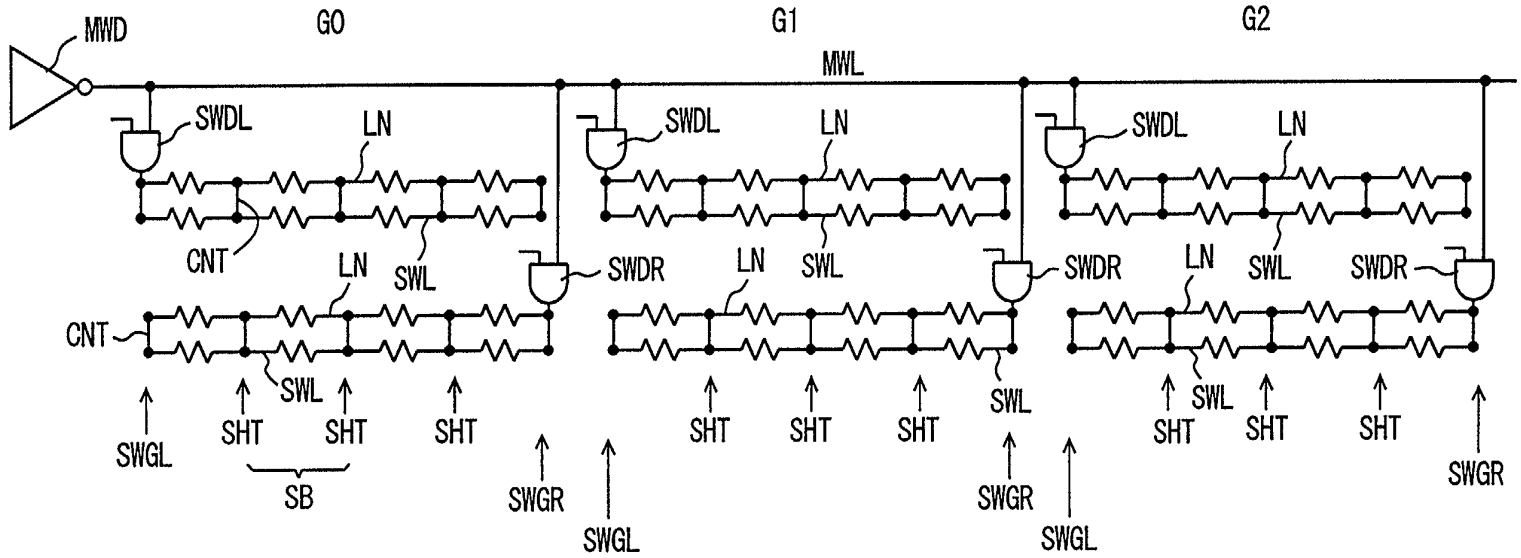

FIG. 16B

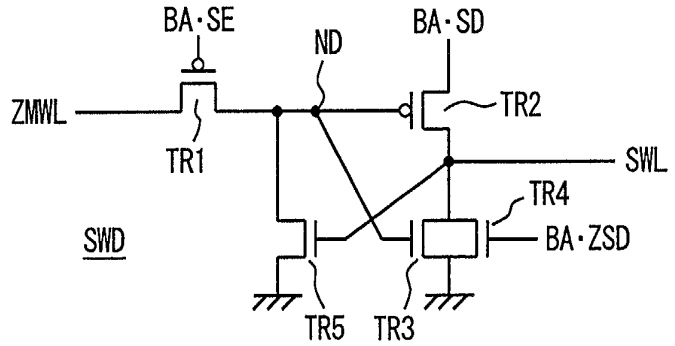

FIG. 17A PRIOR ART

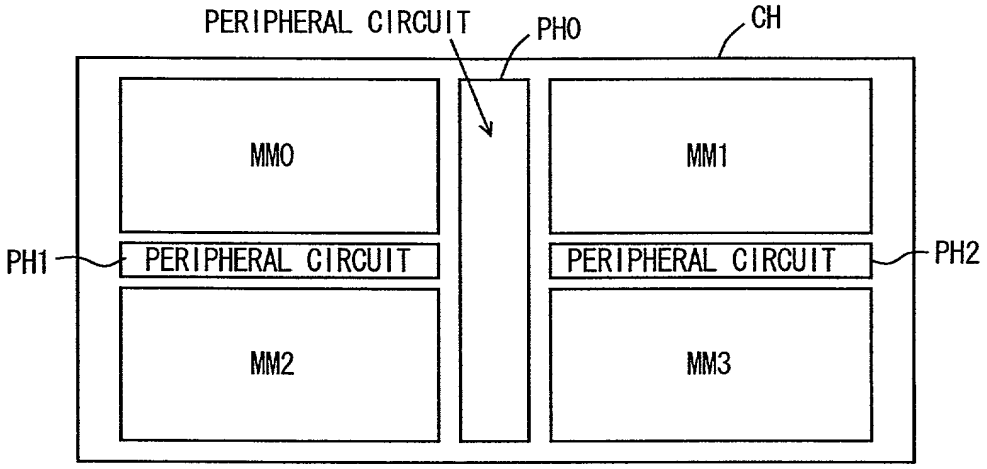

FIG. 17B PRIOR ART

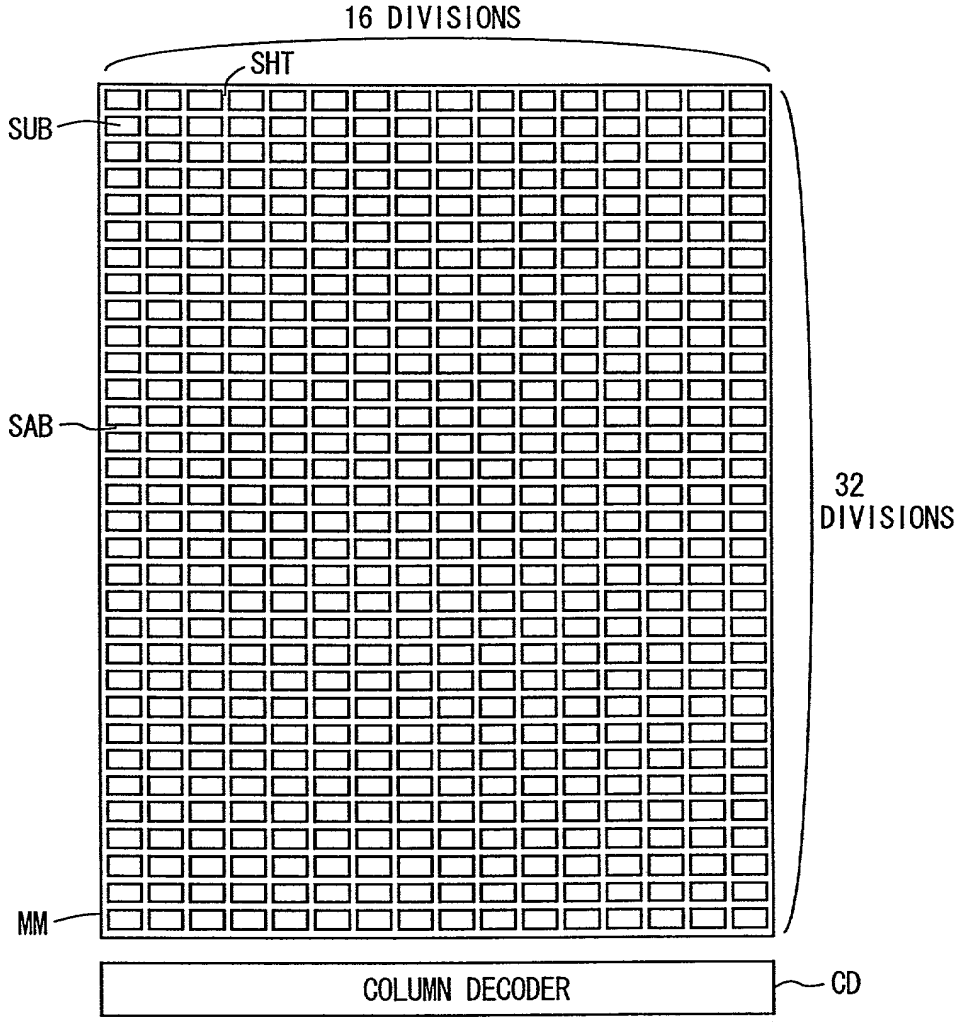

FIG. 18 PRIOR ART

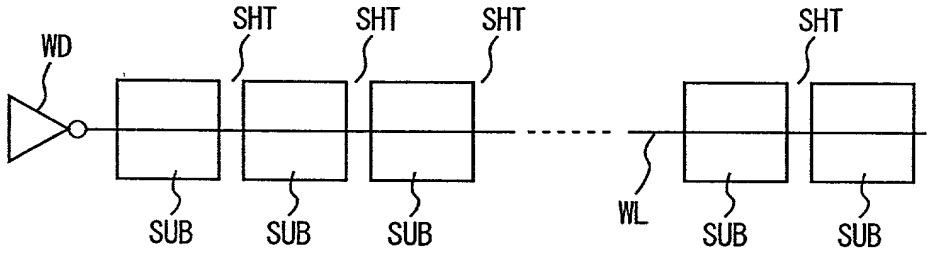

FIG. 19 PRIOR ART

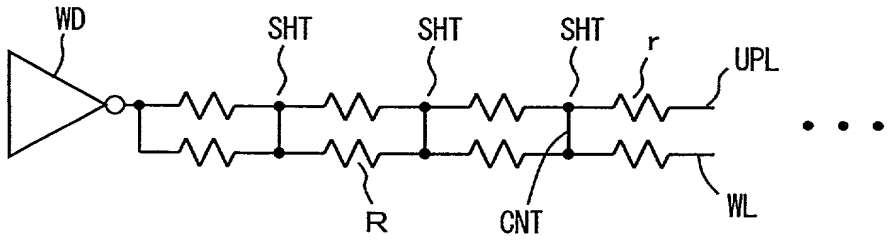

FIG. 20 PRIOR ART

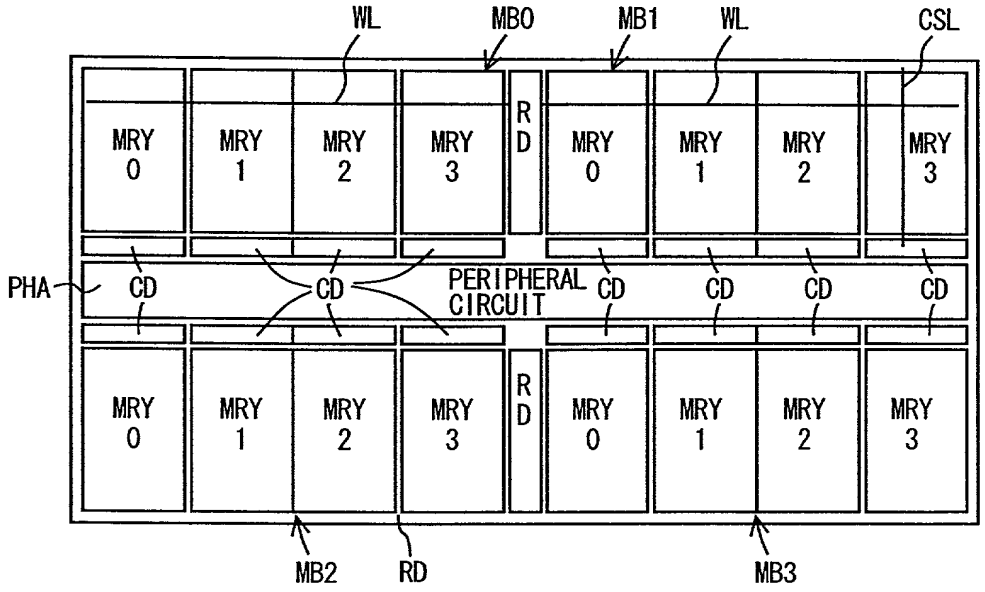

FIG. 21 PRIOR ART

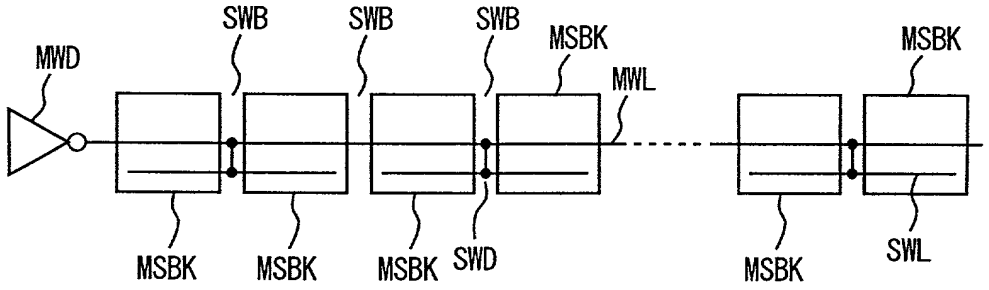

FIG. 22 PRIOR ART

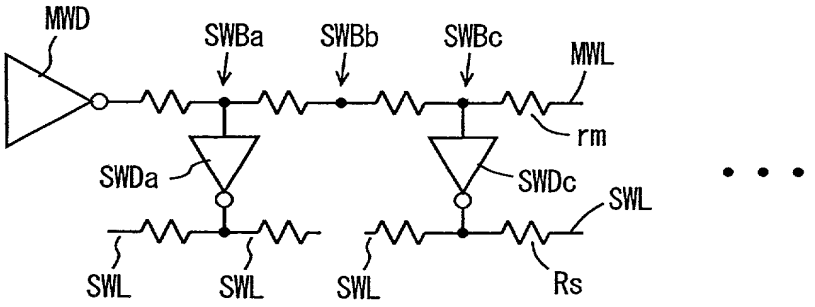

FIG. 23 PRIOR ART

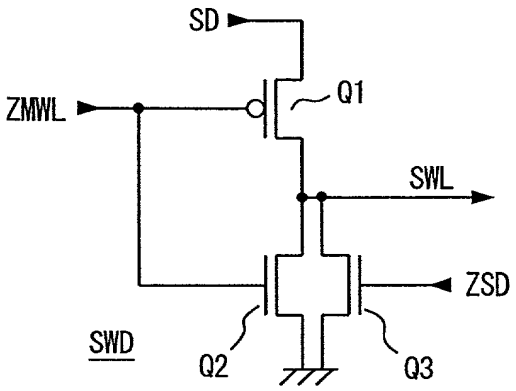
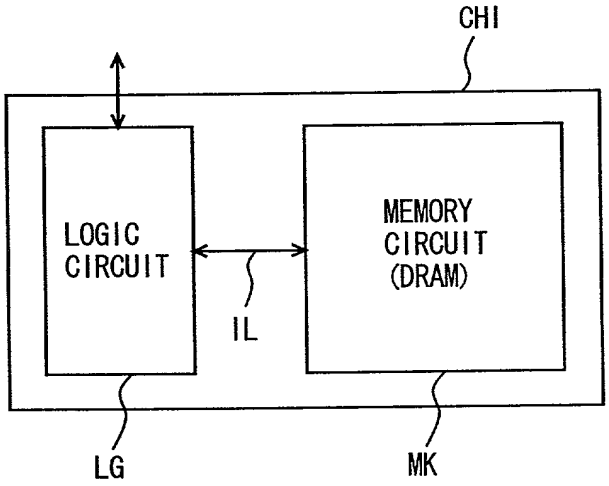
FIG. 24 PRIOR ART